

PHP78NQ03LT

N-channel TrenchMOS logic level FET

Rev. 05 — 9 June 2005

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Logic level threshold
- Fast switching

1.3 Applications

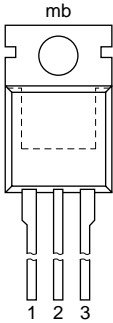
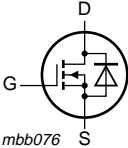
- Computer motherboards
- DC-to-DC converters

1.4 Quick reference data

- $V_{DS} \leq 25\text{ V}$
- $I_D \leq 75\text{ A}$
- $R_{DS(on)} \leq 9\text{ m}\Omega$
- $Q_{GD} = 4.2\text{ nC (typ)}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D)		
3	source (S)		
mb	mounting base; connected to drain		

SOT78 (TO-220AB)

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3. Ordering information

Table 2: Ordering information

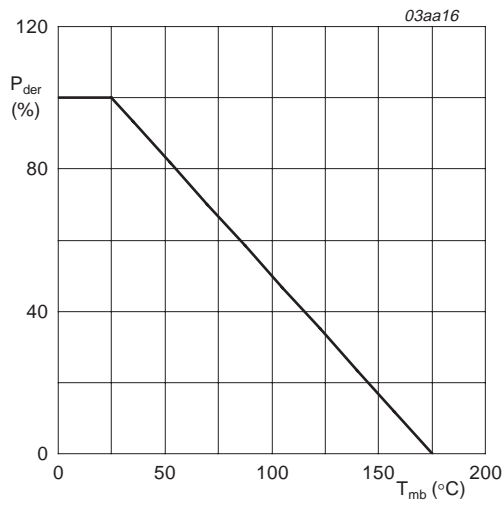
Type number	Package		Version
	Name	Description	
PHP78NQ03LT	SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

Table 3: Limiting values

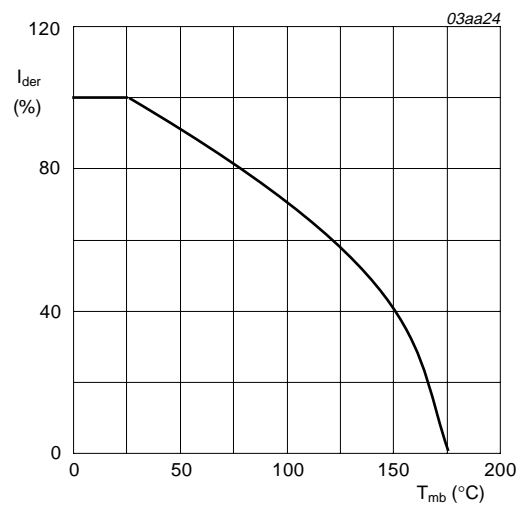
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2 and 3	-	61	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2	-	43	A
		$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$	-	75	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$	-	53	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	228	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	93	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C
Source-drain diode					
I_S	source (diode forward) current	$T_{mb} = 25\text{ °C}$	-	75	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	228	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 43\text{ A}$; $t_p = 0.25\text{ ms}$; $V_{DD} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting at $T_j = 25\text{ °C}$	-	185	mJ



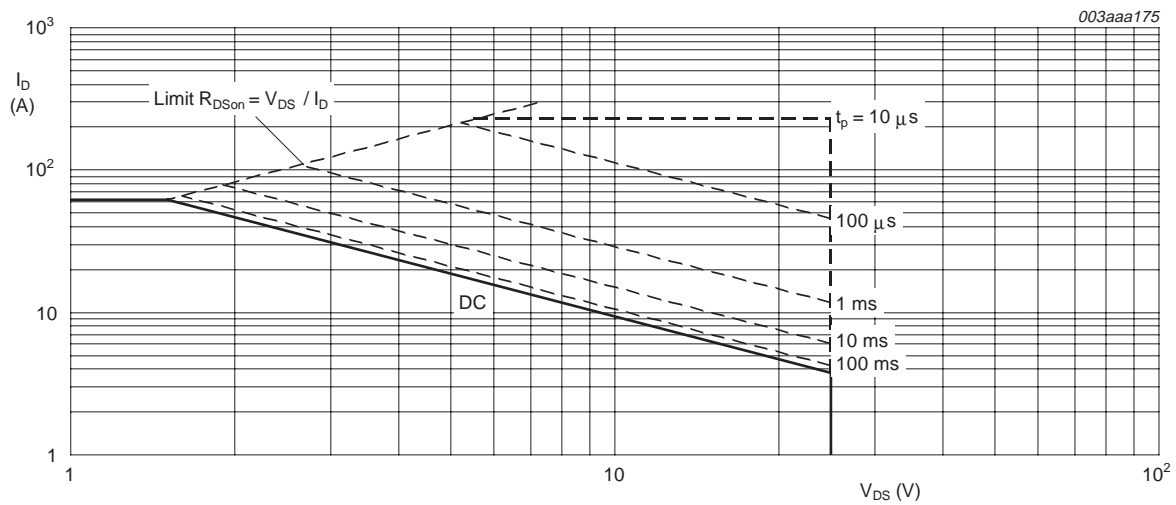
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



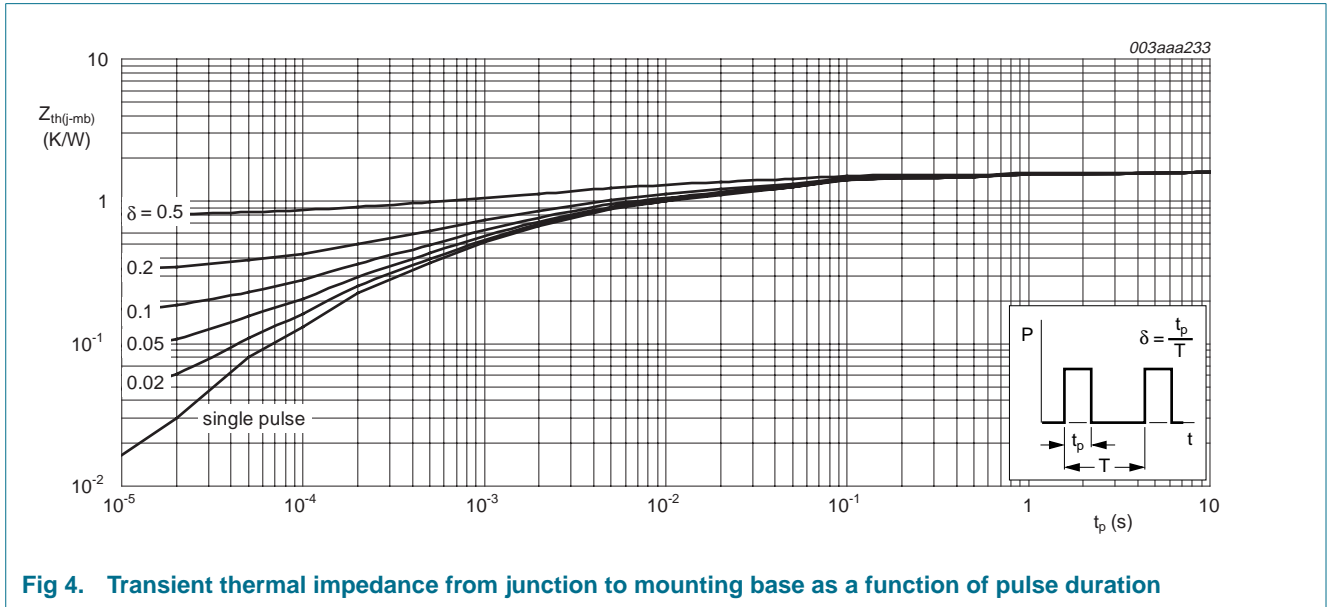
$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse; $V_{GS} = 5 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

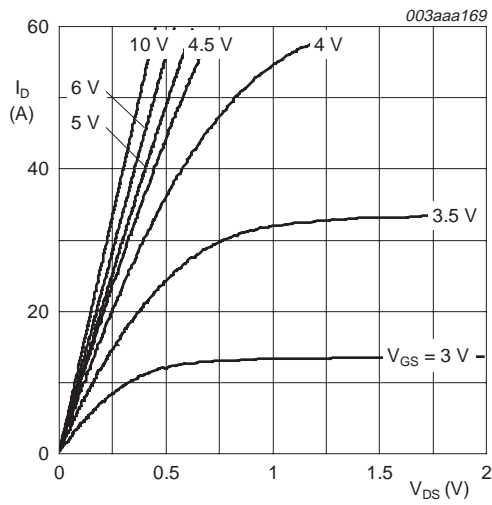
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W



6. Characteristics

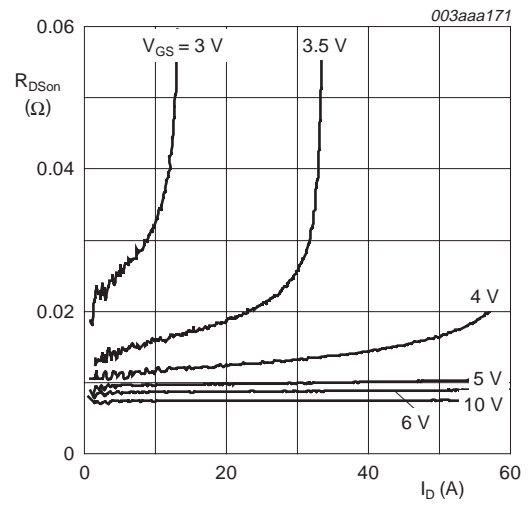
Table 5: Characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V T _j = 25 °C T _j = -55 °C	25 22	- -	- -	V V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9 and 10 T _j = 25 °C T _j = 175 °C T _j = -55 °C	1 0.5 -	1.5 - -	2 - 2.2	V V V
I _{DSS}	drain-source leakage current	V _{DS} = 25 V; V _{GS} = 0 V T _j = 25 °C T _j = 150 °C	- - -	- - -	10 500	μA μA
I _{GSS}	gate-source leakage current	V _{GS} = ±15 V; V _{DS} = 0 V	-	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; Figure 6 and 8 T _j = 25 °C T _j = 175 °C V _{GS} = 10 V; I _D = 25 A; Figure 6 and 8	- - -	11.5 20.7 7.65	13.5 24.3 9	mΩ mΩ mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 50 A; V _{DS} = 15 V; V _{GS} = 5 V; Figure 11	-	13	-	nC
Q _{GS}	gate-source charge		-	4.8	-	nC
Q _{GD}	gate-drain (Miller) charge		-	4.2	5.6	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; Figure 13	-	1074	-	pF
C _{oss}	output capacitance		-	389	-	pF
C _{rss}	reverse transfer capacitance		-	156	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; R _L = 0.6 Ω; V _{GS} = 10 V; R _G = 5.6 Ω	-	20	33	ns
t _r	rise time		-	92	130	ns
t _{d(off)}	turn-off delay time		-	30	48	ns
t _f	fall time		-	40	60	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 12	-	0.95	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V;	-	40	-	ns
Q _r	recovered charge	V _R = 25 V	-	32	-	nC



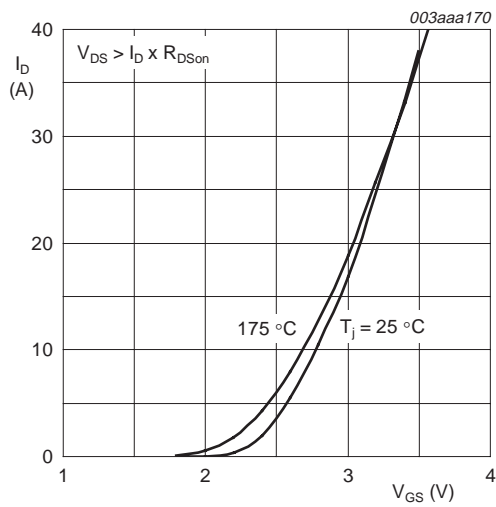
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



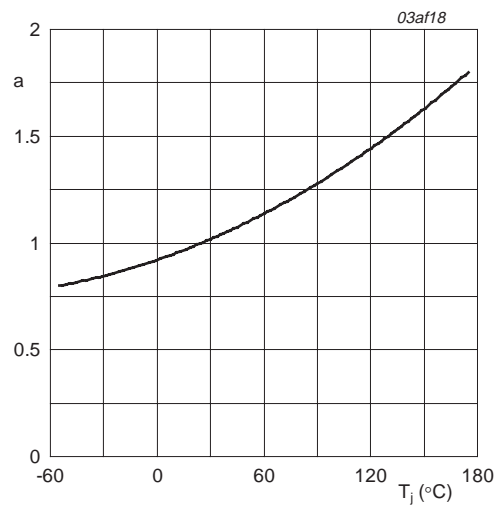
$T_j = 25^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



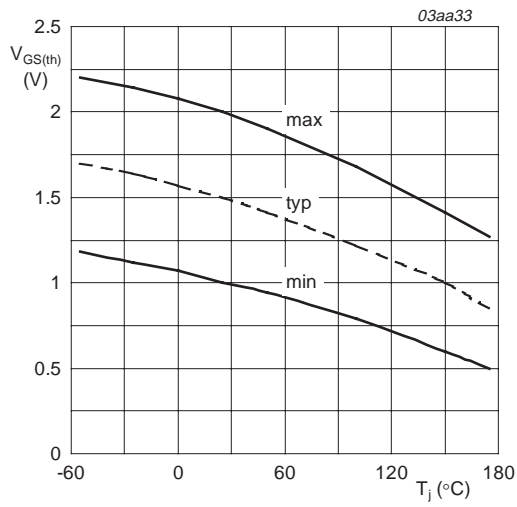
$T_j = 25^\circ\text{C}$ and 175°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



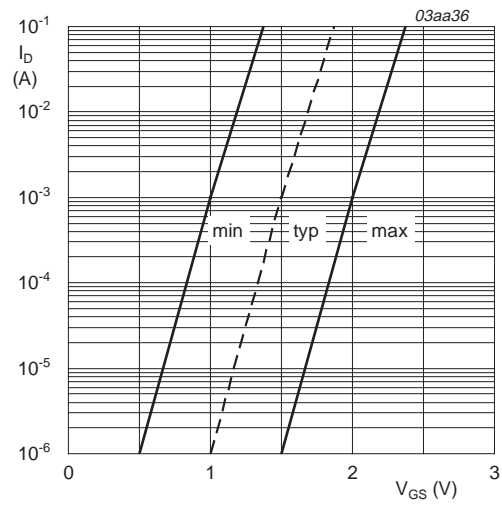
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



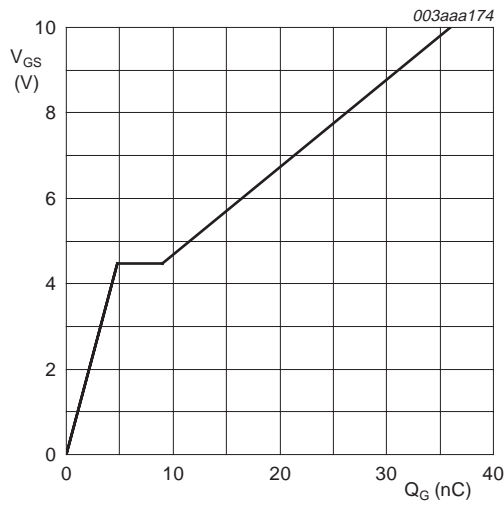
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



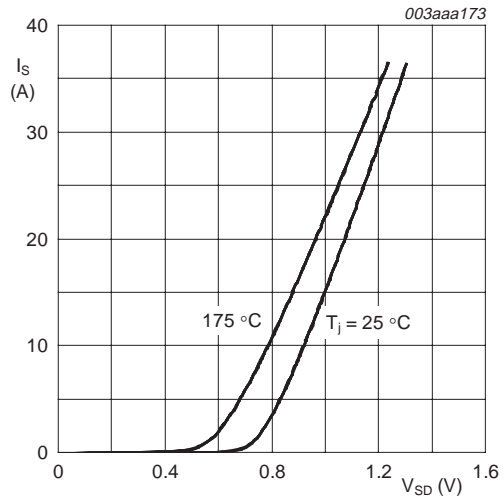
$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



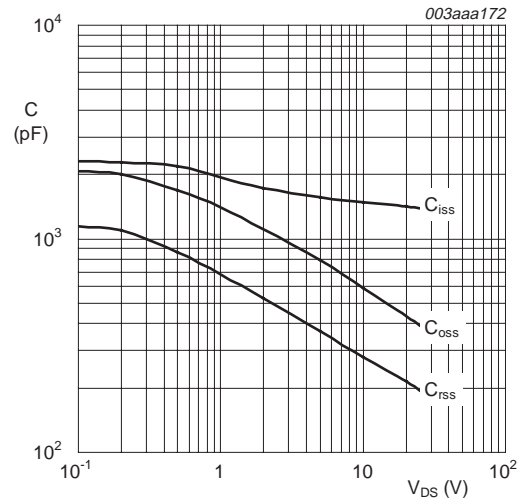
$I_D = 50 \text{ A}; V_{DS} = 15 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$T_j = 25\text{ °C}$ and 175 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



$V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

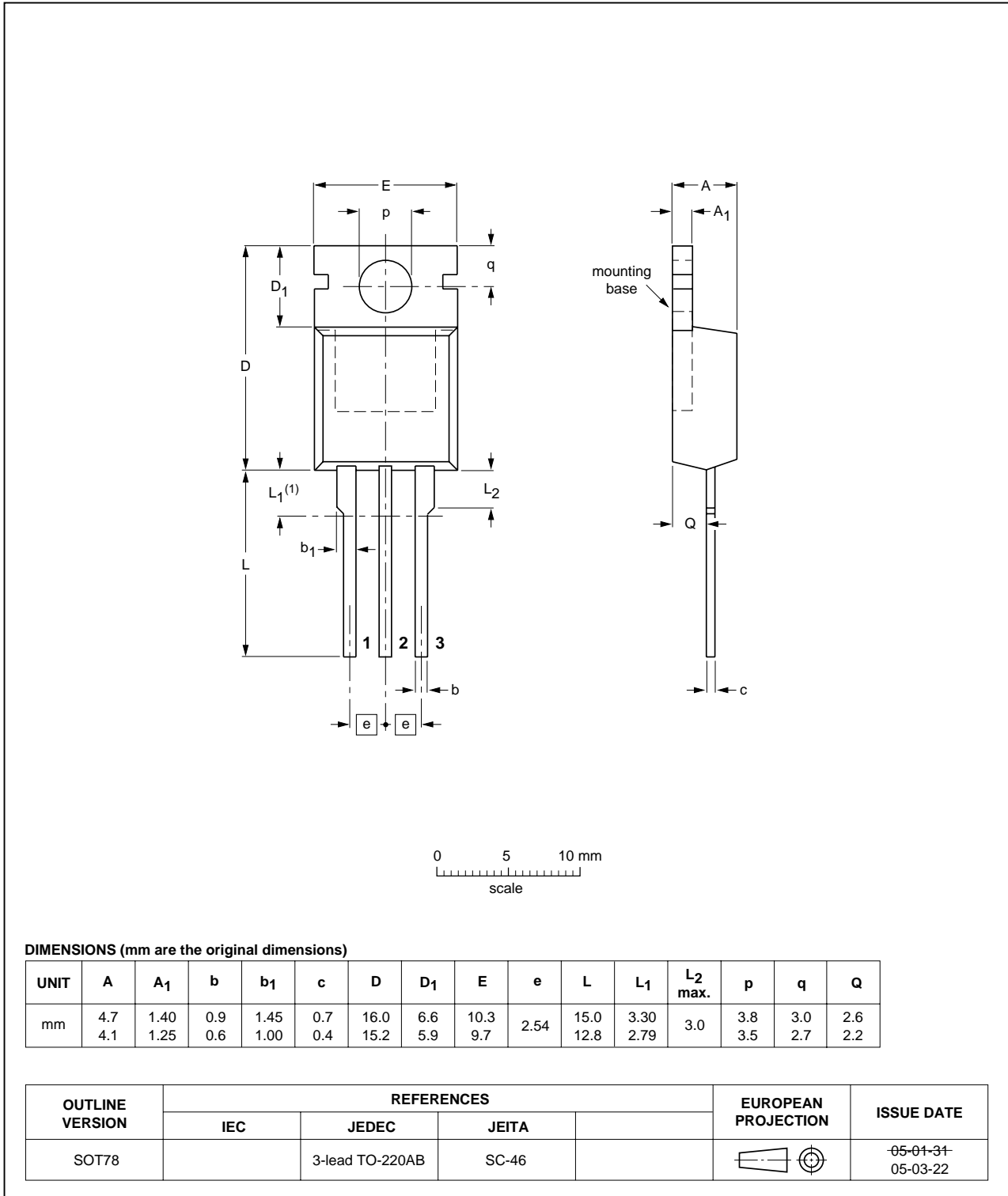


Fig 14. Package outline SOT78 (TO-220AB)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Document number	Supersedes
PHP78NQ03LT_5	20050609	Product data sheet	-	9397 750 15086	PHP_PHU78NQ03LT_4
Modifications:		<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Removal of PHU78NQ03LT (now in separate data sheet). 			
PHP_PHU78NQ03LT_4	20040726	Product data sheet	-	9397 750 13431	PHP_PHB_PHD78NQ03LT_3
PHP_PHB_PHD78NQ03LT_3	20020626	Product data sheet	-	9397 750 09667	PHP_PHB_PHD78NQ03LT_2
PHP_PHB_PHD78NQ03LT_2	20020322	Product data sheet	-	9397 750 09418	PHP_PHB_PHD78NQ03LT_1
PHP_PHB_PHD78NQ03LT_1	20011114	Product data sheet	-	9397 750 08916	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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